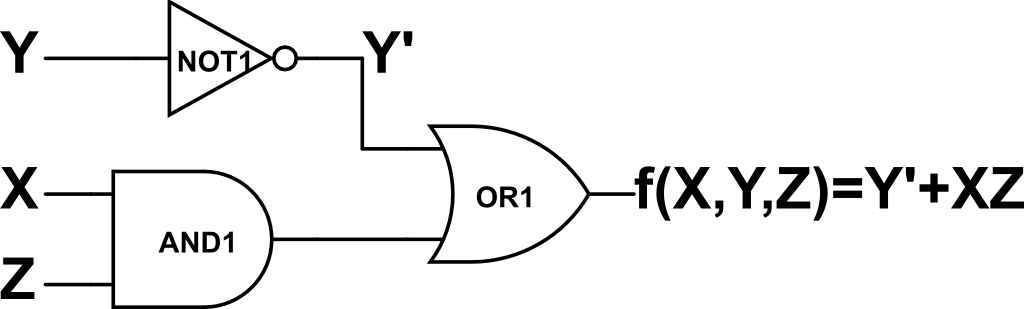
CS 250 2017 Spring Practice Midterm Exam 01 SOLUTION

Purdue University

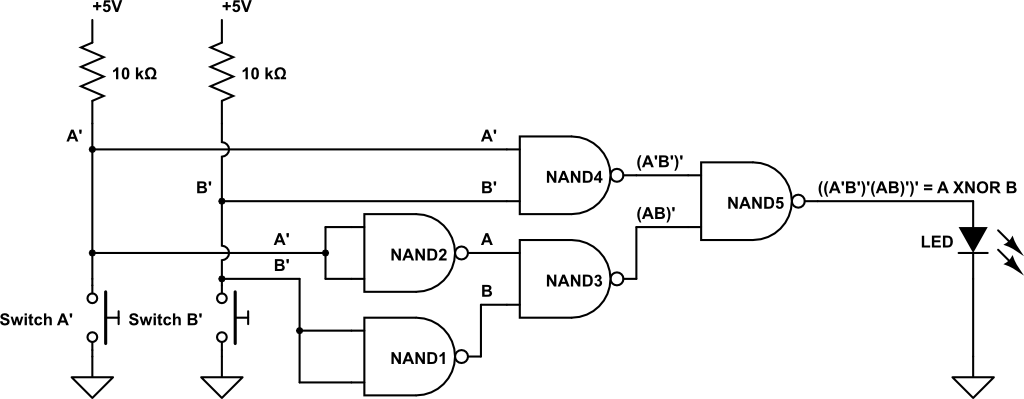
1. Technology change is a significant concern of computer designers and programmers.
   1. **True New technologies change the way we choose to design and program computers.**
   2. False
2. The bit string 01001001 has no meaning.
   1. **True A bit string has no meaning until we define how we will interpret it.**
   2. False
3. The sum of products form of the row A=0 and B=1 for the truth table of the two-input exclusive-OR function is A XOR B.
   1. True
   2. **False The sum of products form requires use of the AND Boolean operation, and the desired term is A'B.**
4. Consider this Karnaugh map for inputs X, Y, and Z.

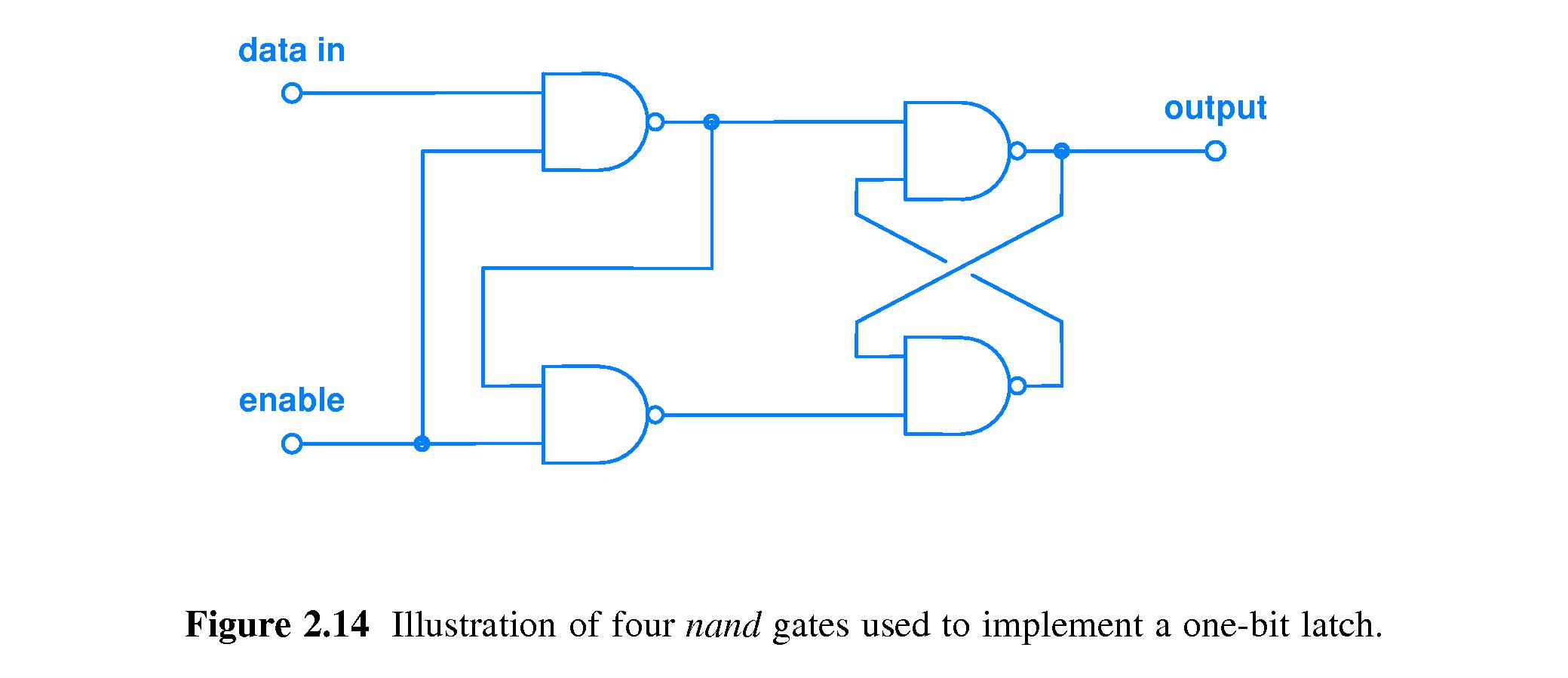
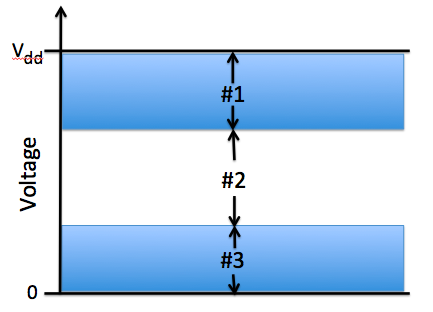
|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| f(X,Y,Z) | XY = 00 | XY = 01 | XY = 11 | XY =10 |
| Z = 0 | 1 | 0 | 0 | 1 |
| Z = 1 | 1 | 0 | 1 | 1 |

Assume that you have access only to X, Y, and Z, so if you want Z’, your circuit must compute it. A minimal sum of products circuit to implement this truth table has

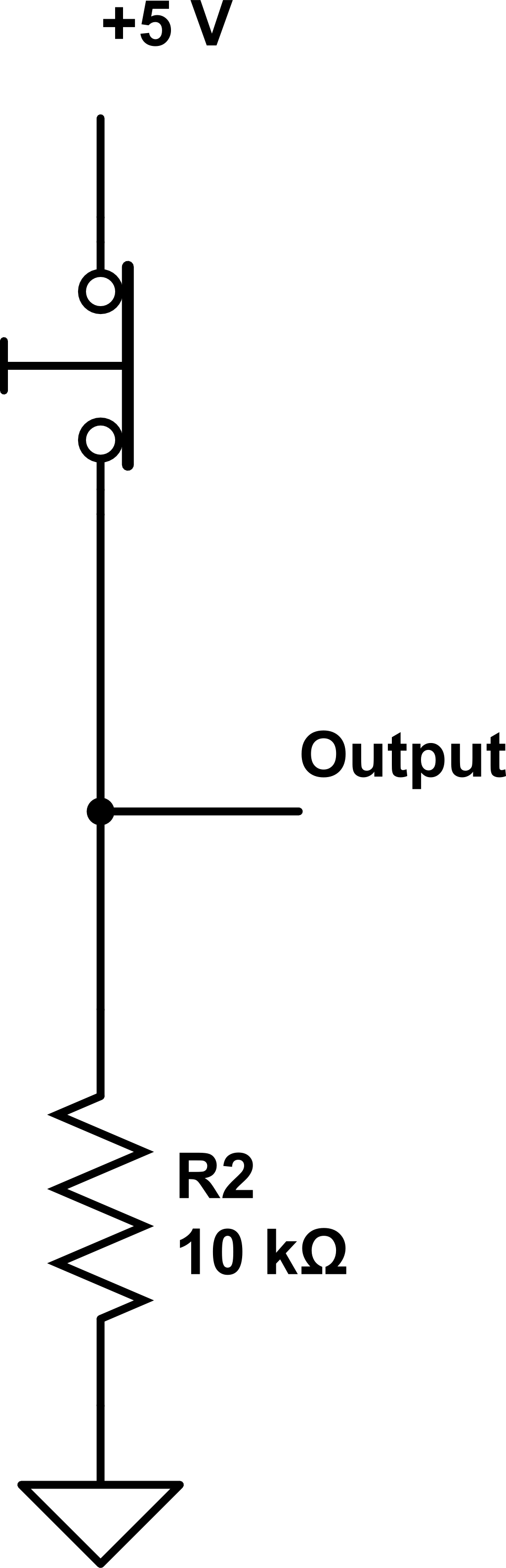
* 1. Two two-input NAND gates and a two-intput NOR gate
  2. **One two-input AND gate, one two-input OR gate, and one NOT gate**
  3. One four-input NAND gate and an inverter
  4. Five two-input NAND gates
  5. None of the above answers is correct  
       
     Grouping 4 ones from the left and right columns yields the product term Y’. Grouping the final one with the one in the lower right corner yields the term XZ. So the SOP equation is f(X,Y,Z) = Y’ + XZ and the circuit is  
     

1. When software would use iteration to carry out a repetitive task, hardware uses
   1. An increase in supply voltage
   2. **Replication** Consider how multiple bit numbers can be added by stringing together copies of the full adder.
   3. Higher speed gates
   4. Exclusive-Or gates
   5. None of the above
2. To point to one of 32 locations requires
   1. A multiplexer
   2. **A 5-bit string** A multiplexer can be said to point, but it also has the ability to transfer data, so a multiplexer is more than what is required. A 5-bit string can point to 25 locations, or 32. More than 5 bits, answer C, is not required by virtue of being excessive. A decoder with 32 (address bits) inputs can point to 232 locations, far more than required here.
   3. A 32-bit pointer
   4. A decoder with 32 inputs
   5. None of the above is necessary
3. The truth table for a 4-bit adder made from full adders has how many rows?
   1. 4
   2. 16
   3. 256
   4. 2256
   5. **None of the above** The inputs to a 4-bit adder made from full adders are 4 bits of addend, 4 bits of augend, and 1 bit of carry in. The answer of 29 rows or 512.
4. Which adder circuit type can be operated the fastest assuming that all gate delays are equal and all wire propagation delays are equal?
   1. 1’s complement
   2. **2’s complement** 2’s complement avoids the end around carry required of 1’s complement
   3. 1’s and 2’s complement are equally fast
   4. Because 1's complement is faster than 2’s complement for some (addend, augend) pairs and not for other pairs, it is incorrect to say that one of these adder types can be operated faster than the other.
   5. None of the above answers is correct.
5. Which of the following expressions and notations represents or corresponds to the most negative value possible for an 8-bit 2’s complement number?
   1. 11111111
   2. **0x80** The most negative 8-bit 2’s complement number has the form 1000 0000, with a space added for readability. It’s value is -27 or -128.
   3. – (27 – 1) This is the most negative value possible with 8-bit 1’s complement.
   4. – (28 – 1)
   5. None of the above answers is correct
6. The bit string 1001000000010101 could be a packed BCD value.
   1. **True** This string is 0x9015 representing the decimal integer 9,015.
   2. False

Consider the circuit below, which was constructed for Lab 01, when answering the two questions that follow.  
  


1. The operation of this circuit will be unchanged if a 2-input NOR gate is substituted for NAND1 and no other change is made.
   1. **True** A 2-input nor with its inputs tied together also functions as an inverter, matching the function of NAND1 in this circuit.
   2. False
2. The operation of this circuit will be unchanged if the 10 kΩ resistors are replaced with zero ohm resistors.
   1. True
   2. **False** If the 10 kΩ resistors are replaced with 0 Ω resistors, then the voltage divider circuit pairs two essentially zero ohm devices, the new resistors and the NO SPST push-button switches. The logic 0 function of these inputs will be compromised and there will be a zero ohm path from power to ground when either switch is pushed (closed), also not good due to excessive current that will from power to ground in this case.
3. Consider Figure 2.14 from the textbook.  
     
   Let t be the initial time this circuit is examined. Which statement is true?
   1. If at time t enable = 1 and data in = 0 and are held constant, then output(t) = 0 and output(t+1) = 0
   2. If at time t enable = 1 and data in = 0 and are held constant, then output(t) = X and output(t+1) = 1
   3. If at time t enable = 0 and data in = 1 and are held constant, then output(t) = X and output(t+1) = 1
   4. **None of the statements A, B, and C are true** Statement A would be true if is said that output(t) = X. Statements B gets the value of output(t+1) wrong. Statement C, where enable = 0 should have output(t+1) = output(t), i.e., no change.
4. For 8-bit sign-magnitude and 1’s complement representations of the decimal value -3, in how many bit positions do these two representations differ?
   1. 1
   2. 3
   3. 5
   4. **7** Sign-magnitude for -3 is 1000 0011 with a space added for readability. For 1’s complement -3 is the bitwise inverse of 0000 0011 or 1111 1100. These representations differ in all but the sign bit, so they differ in 7 bit positions.
   5. None of the above
5. A digital logic circuit that given an input bit string X computes an output Y and then, later, given the same input bit string X computes a different output Z must contain
   1. A counter
   2. A NOT gate
   3. **A latch** The output of this circuit is not the same for each identical input, therefore this is not a combinatorial circuit that is computing based only on the current inputs. Rather, this must be a sequential circuit that can behave differently depending on its accumulated history of operation. Answers A, B, D, and E are combinatorial circuits where outputs are an unchanging function of inputs. The only sequential circuit choice among the answers is the latch. Every sequential circuit contains at least one latch.
   4. An adder
   5. A decoder
6. A function in a program produces a result only after it has been called. Hardware, upon receiving power, produces an output signal immediately and at all time thereafter, no matter how many gate delays circuit input signals must propagate through on the longest path to a circuit output.
   1. **True** The output signals of hardware start generating output logic values the moment that power is given. These outputs may well not reflect the current inputs, but that is for the circuit designer and the programmers to allow for.
   2. False
7. What fraction of the possible input values yield Sum = 0 and Carry out = 1 for a full adder?
   1. 1/8
   2. 2/4
   3. **3/8** The ways to produce the specified outputs are (addend, augend, carry in) of (1,1,0), (1,0,1), and (0,1,1). These are three of eight possible input combinations of three input bits.
   4. 4/16
   5. 5/8
8. 24 bytes is 4 times as many bytes as is 20 (base 16) bits.
   1. **True** 24 bytes = 24 x 23 bits = 27 bits. 20 base 16 = 2x161+0x160 = 32 = 25. The ratio of 27 to 25 is 22 = 4.
   2. False
9. Which of the following is one of DeMorgan’s Laws?
   1. (X’)’ = X
   2. **(AB)’ = A’ + B’**
   3. (C’D’) = C’ + D’
   4. (Y + Z)’ = Y’ + Z’
   5. None of the above is one of DeMorgan’s Laws
10. Memory locations are pointed to by hardware. Designing a computer with four times more memory than specified in the original design requires
    1. Using one more address bit
    2. **Using two more address bits** Each additional address bit doubles the number of locations that can be pointed to.
    3. Using four more address bits
    4. Using four times the number of address bits
    5. None of the above
11. Consider the following diagram showing three voltage bands labeled #1, #2, and #3.  
      
      
    Which band, or which combination of bands, guides us in designing digital computer circuits where the logic gate input signal voltage levels need not be perfect yet gate operation will be digital, not analog?
    1. #1
    2. #1 and #2
    3. #2
    4. #2 and #3
    5. **None of the above answers is correct** The correct answer is bands #1 and #3.

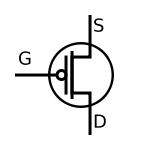
|  |  |  |
| --- | --- | --- |
| A | B | f(A,B) |
| 0 | 0 |  |
| 0 | 1 |  |
| 1 | 0 |  |
| 1 | 1 |  |

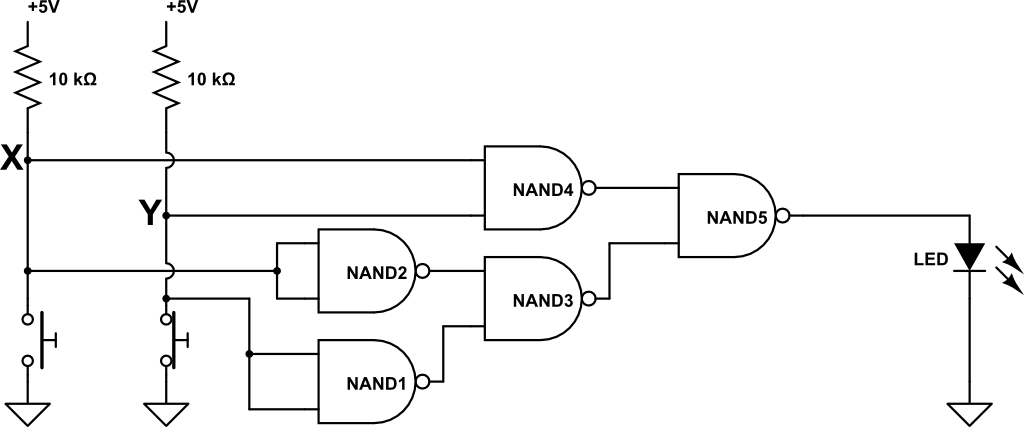
1. Consider the following truth table.  
     
     
     
     
     
     
     
   The missing truth table entries, in order from top to bottom, could be
   1. 0 0 1 0 if f(A,B) = (A + B) modulo 2 [A+Bmod 2 entries would be 0110]
   2. 0 1 1 0 if f(A,B) = A XNOR B [A XNOR B entries would be 1001]
   3. **1 0 0 0 if f(A,B) corresponds to a universal logic gate** Because 1000 corresponds to A NOR B and NOR is a universal gate.
   4. 0 0 0 1 if f(A,B) corresponds to a universal logic gate [0001 is AND which is not universal]
   5. X 1 0 X if f(A,B) = A’ [for A’ the table would be 1100]
2. The binary string 1010, when interpreted as a 2’s complement number represents the decimal number value
   1. 10
   2. -2
   3. -5
   4. **-6**
   5. None of the above
3. Consider this circuit to generate a digital input.  
     
     
   1. **This input circuit is an active low design**
   2. This input circuit is fine for use with digital logic circuits of every type [This input bounces, so it is inappropriate as an input to an edge-triggered digital logic circuit.]
   3. We cannot say whether this input circuit is active high or not until information about whether the switch is being pushed is given to us [See lecture slides on high-active, low-active]
   4. This circuit will work only when we exchange the positions of the switch and the resistor in the circuit, that is, put the switch where the resistor is shown and put the resistor where the switch is shown [This circuit works fine as is. A related variant of this circuit can be built as described.]
   5. This design would be improved if R2 had the value 470 ohms [470 ohms will make for a poorer voltage divider. Do the math to determine the quality of the low level and high level voltage outputs in comparison to the two voltage levels produced when he resistor is 10,000 ohms.]
4. The reason we prefer to build digital logic circuits to operate in base 2 rather than base 10 is
   1. Cost
   2. Speed
   3. Easier to manufacture
   4. **Any of the above** Each of characteristics A, B, and C is ﻿﻿﻿﻿﻿﻿﻿﻿improved by choosing base 2 instead of base 10.﻿﻿﻿﻿﻿﻿﻿﻿
   5. None of the above
5. Each possible combination of inputs is applied to both a 2-input NAND gate and a 2-input XOR gate, and the outputs of the two gates are compared. How many times will the outputs of these two gates be the same?

A 0 B 1 C 2 D 3, for input combinations 01, 10, and 11 E 4

1. The amount of time needed by a combinatorial circuit to complete its computation is
   1. **measured in units of gate delays.**
   2. essentially zero because logic gates produce an output voltage as soon as they receive power. – computation is not yet complete
   3. is unpredictable. – false, the propagation delay of a given circuit can be known.
   4. Is all of the above answers
   5. is none of the above answers.
2. Fill in the table to show how the following 32-bit binary string (byte boundaries are indicated by space for convenience) 00001111 10101100 11110000 10011010  
   will be stored in computer memory assuming Little Endian byte order.

|  |  |
| --- | --- |
| Addressable Memory Location Number | Little Endian Solution (least significant byte goes into the lowest memory address) |
| *k* | 10011010 |
| *k* + 1 | 11110000 |
| *k* + 2 | 10101100 |
| *k* + 3 | 00001111 |

1. Why is a biased exponent representation used by the IEEE Floating Point Standard?  
   **Answer:** It makes alignment of mantissas easy because the bias translates the allowed range of positive and negative exponent values to the same range of unsigned (i.e., positive) integers, thereby translating the comparison of two exponents into a comparison of two unsigned integers, an easier comparison than comparing signed numbers.
2. In Figure 2.3 of the textbook, which transistor turns on when the input is a low voltage?  
   **Answer:**   
   
3. The 4-bit unsigned integers 1010 and 0110 are added. What should be the output of a well-designed ALU?  
   **Answer:** A result of 0000 and an Overflow signal.
4. Draw a voltage waveform that has one falling edge.  
   Answer: \_\_\_\_\_\_\_\_\_\_  
    \\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_
5. Consider the schematic below for the following questions.



* 1. Using the given names of any relevant signals shown in the schematic, what is the Boolean expression for the output of gate NAND4?

(XY)’

* 1. Is the LED **on** or **off** or **cannot determine with the given information**?

By the way the two pushbutton switches are drawn, X = 5 volts and Y = 0 volts, so X=1 and Y=0 and the circuit computes X XNOR Y = 1 XNOR 0 = 0. So, the voltage at the output of NAND5 is low, so the LED is off.

1. What principle allows for the simplification of descriptions of hardware by omission of unimportant detail?  
   **Answer:** Abstraction.